Workshop on Wide Bandgap Bipolar Devices

MEETING PROGRAM & ABSTRACT BOOK

25-28 January 1999
Marriott Bay Point Resort Village
Panama City Beach, FL

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REPORT DOCUMENTATION PAGE

Form Approved
OMB No. 0704-0188

Public reporting burden for this collection of information is estimated to average 1 hour per response, including the time for reviewing instructions, searching data sources, gathering and maintaining the data needed, and completing and reviewing the collection of information. Send comments regarding this burden estimate or any other aspect of this collection of information, including suggestions for reducing this burden to Washington Headquarters Service, Directorate for Information Operations and Reports, 1215 Jefferson Davis Highway, Suite 1204, Arlington, VA 22202-4302, and to the Office of Management and Budget, Paperwork Reduction Project (0704-0188) Washington, DC 20503.

PLEASE DO NOT RETURN YOUR FORM TO THE ABOVE ADDRESS.

1. REPORT DATE *(DD-MM-YYYY)*	2. REPORT DATE Type	3. DATES COVERED *(From - To)*
29-07-99	Final - Technical	01/01/1999 to 30/06/1999

4. TITLE AND SUBTITLE

Workshop on Wide Bandgap Bipolar Devices

5a. CONTRACT NUMBER

N00014-99-1-0026

5b. GRANT NUMBER

N00014-99-1-0026

5c. PROGRAM ELEMENT NUMBER

6. AUTHOR(S)

5d. PROJECT NUMBER

5e. TASK NUMBER

5f. WORK UNIT NUMBER

7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES)

The Minerals, Metals & Materials Society, Inc.
184 Thorn Hill Road
Warrendale, PA 15086

8. PERFORMING ORGANIZATION REPORT NUMBER

9. SPONSORING/MONITORING AGENCY NAME(S) AND ADDRESS(ES)

10. SPONSOR/MONITOR'S ACRONYM(S)

11. SPONSORING/MONITORING AGENCY REPORT NUMBER

12. DISTRIBUTION AVAILABILITY STATEMENT

Approved for public release

13. SUPPLEMENTARY NOTES

A proceedings was not published. The attached is the Meeting Program and Abstract Book for this Workshop.

14. ABSTRACT

15. SUBJECT TERMS

16. SECURITY CLASSIFICATION OF:			17. LIMITATION OF ABSTRACT	18. NUMBER OF PAGES	19a. NAME OF RESPONSIBLE PERSON
a. REPORT	b. ABSTRACT	c. THIS PAGE		1	Alexander R. Scott
					19b. TELEPONE NUMBER *(Include area code)* 724-776-9000

Workshop on Wide Bandgap Bipolar Devices

	Speaker Name/Paper Title
Session 1: Monday AM 25 January 1999 (9:20 am - Noon)	**ST. ANDREWS BALLROOM SALON V**
7:45 a.m. - 8:30 a.m. - Registration and Continental Breakfast	
8:30 a.m. - Welcome & Orientation	
8:40 a.m. - 9:10 a.m. (Scene-setter)	***Umesh Mishra*** - AlGaN/GaN HBTs: Status and Potential
9:10 a.m. - 9:30 a.m.	***John Torvik*** - GaN/SiC Heterojunction Bipolar Transistors
9:30 a.m. - 9:50 a.m.	***Robert Hickman*** - GaN NPN Junction Issues & Developments
9:50 a.m. - 10:10 a.m.	***William Schaff*** - GaN/SiC HBTs
Break: 10:10 a.m. - 10:30 a.m.	
10:30 a.m. - 11:00 a.m. (Scene-setter)	***Ilesanmi Adesida*** - Processing for GaN-based Heterojunction Bipolar Transistors
11:00 a.m. - 11:20 a.m.	***Bart Van Zeghbroeck*** - GaN/SiC HBTs and Related Topics
11:20 a.m. - 11:40 a.m.	***Mark Rodwell*** - Prospects for Wide Bandwidth Transferred Substrate Power HBTs
11:40 a.m. - 12:00 noon	***Erhard Kohn*** - Prospects of Diamond Bipolar Devices
Lunch: 12:00 noon - 1:00 p.m.	**GRAND LAGOON BALLROOM A&B**
Session 2: Monday PM (7:00 p.m. - 9:00 p.m.)	**ST. ANDREWS BALLROOM SALON V**
7:00 p.m. - 7:30 p.m. (Scene-setter)	***Peter Asbeck*** - Enhancement of Base Conductivity via the Piezoelectric Effect in AlGaN/GaN Heterojunction Bipolar Transistors
7:30 p.m. – 7:50 p.m.	***Tom McGill*** - The Values of Minority Carrier Lifetime and Their Implications for Bipolar Devices
7:50 p.m. - 8:10 p.m.	***Russ Dupuis*** - Design and Simulation of AlGaN/GaN Heterojunction Bipolar Transistors
Break: 8:10 p.m. - 8:20 p.m.	
8:20 p.m. - 8:50 p.m. (Scene-setter)	***Kevin Brennan*** - Materials Theory Based Modeling of Wide Band Gap Semiconductors: From Basic Properties to Devices
8:40 p.m. - 9:00 p.m.	***D. Pavlides*** - DC and High-Frequency Characteristics of GaN-based Heterojunction Bipolar Transistors
9:00 p.m. - 9:20 p.m.	***M. Wojtowicz*** - GaN HBT Design and Optimization
Session 3: Tuesday AM (8:30 am - 12:00 noon)	**ST. ANDREWS BALLROOM SALON V**
7:45 a.m. - 8:30 a.m. - Continental Breakfast	
8:30 a.m. - 9:00 a.m. (Scene-setter)	***Paul Chow*** - SiC and GaN High-Voltage Power Devices
9:00 a.m. - 9:20 a.m.	***Ravi Kirin Chilukuri*** - Characteristics of 10kV Planar ACBTs in 4H-SiC
9:20 a.m. - 9:40 a.m.	***Anant Agarwal*** - SiC Gate Turnoff Thyristors for High Power, High Temperature Applications
9:40 a.m. - 10:00 a.m.	***Pankaj Shah*** - Indepth Analysis of SiC GTO Thyristor Device Performance Using Numerical Simulations
Break 10:00 a.m. - 10:20 a.m.	
10:20 a.m. - 10:40 a.m.	***John Palmour*** - SiC Bipolar Devices - Potentials & Limits (Part 1 of 2)
10:40 a.m. - 11:00 a.m.	***Ranbir Singh*** - SiC Bipolar Devices - Potentials & Limits (Part 2 of 2)
11:00 a.m. - 11:20 a.m.	***Manfred Frischholz*** - Recent Development in SiC High Voltage Rectifiers
11:20 a.m. - 11:40 a.m.	***Jian Zhao*** - Fabrication and Characterization of 4H-SiC GTOs
11:40 a.m. - 12:00 noon	***Nicole Krishnamurthy*** - Progress on SiC Bipolar Power Devices
Lunch: 12:00 noon - 1:00 p.m.	**GRAND LAGOON BALLROOM A&B**
Reception: 7:00 - 7:30 p.m.; Banquet: 7:30 p.m. - 9:00 p.m.	**ST. ANDREWS BALLROOM SALON V**

	Speaker Name/Paper Title
Session 4: Wednesday AM (8:30 am - 12:00 noon)	**GRAND LAGOON BALLROOM F&G**
8:15 a.m. - 9:00 a.m. - Continental Breakfast	
9:00 a.m. - 9:20 a.m.	***Suzanne Mohney*** - Ohmic Contacts to p-Type GaN and SiC
9:20 a.m. - 9:40 a.m.	***Mike Barsky*** - GaN Etching Techniques
9:40 a.m. - 10:00 a.m.	***Marvin White*** - An Improved Inversion-Mode 6H-SiC DIMOS Power Transistor
10:00 a.m. - 10:20 a.m.	***Jim Cooper*** - State-of-the-Art of SiC MOSFETs as an Alternative to Bipolar Devices for Power Switching Applications
Break: 10:20 a.m. - 10:40 a.m.	
10:40 a.m. - 11:00 p.m.	***Mike Mazzola*** - Advanced Heteroepitaxy of Silicon Carbide on Silicon.
11:00 a.m. - 11:20 a.m.	***Gerhard Wachutka*** - Electrothermal Analysis of SiC Power Devices Using Physically-Based Device Simulation
11:20 a.m. - 11:40 a.m.	***Alex Huang*** - Comparing 4H-SiC Power Switching Devices: UMOS, Hybrid JFET, GTO and NPN Transistor
11:40 a.m. - 12:00 noon	***Anant Agarwal*** - Status and Prospects of SiC SITs
Lunch: 12:00 noon - 1:00 p.m.	**GRAND LAGOON BALLROOM A&B**
Session 5: Wednesday PM (1:00 p.m. - 4:50 p.m.)	**GRAND LAGOON BALLROOM F&G**
1:00 p.m. - 1:30 p.m. (Scene-setter)	***Cammy Abernathy*** - Fabrication of 300° C GaN/AlGaN Heterojunction Bipolar Transistors
1:30 p.m. - 1:50 p.m.	***April Brown*** - GaN Growth on Lithium Gallate Substrates
1:50 p.m. - 2:10 p.m.	***Michael Shur*** - Two Dimensional Hole Gas Induced by Piezoelectric and Pyroelectric Charges
2:10 p.m. - 2:30 p.m.	***Larry Rowland*** - Materials Challenges for p+ SiC-based GaN/Sic HBTs
2:30 p.m. - 2:50 p.m.	***Michael Topf*** - GaN/SiC Heterojunctions Grown by LP-CVD
Break: 2:50 p.m. - 3:10 p.m.	
3:10 p.m. - 3:30 p.m.	***Andrew Steckl*** - Growth and Application of Thick 3C-SiC Films on Si
3:30 p.m. - 3:50 p.m.	***Alan Doolittle*** - The Characterization of GaN and SiC Materials for Minority Carrier Device Applications
3:50 p.m. - 4:10 p.m.	***John Zolper*** - Opportunities for Wide Bandgap Bipolar Devices in Navy Systems
4:10 p.m. - 4:30 p.m.	***Thomas Jenkins*** - Air Force Needs: The Technical Challenges of Wide Bandgap Bipolar Devices for Air and Space Sensors
4:30 p.m. - 4:50 p.m.	***Colin Wood*** - Roadblocks to Wide-Gap Bipolars
Wrap-up Session/Continental Breakfast: Thursday AM - 28 January - (8:00 am - 11:00 am) **ST. ANDREWS BALLROOM SALON V**	

AlGaN/GaN HBTs: Status and Potential

Umesh K. Mishra (and unfortunate colleagues, Lee McCarthy, Jae Limb, Andreas Stonas, Peter Kozodoy, Yulia Smortchkova, Stacia Keller, Evelyn Hu, Mark Rodwell, Jim Speck and Steve DenBaars)

The advantages offered by AlGaN/GaN HBTs are

1. The high breakdown voltage in the GaN collector offers high voltage operation
2. The excellent electron velocity-field characteristics in GaN promises low collector transit time.
3. The large band gap change with grading provides a large drift field in the base reducing base transit time.
4. The ease of contacts to n GaN reduces emitter and collector contact resistance.

The only disadvantage is that the electronic properties of p-GaN which constitutes the base are currently poor, resulting in a high base resistance caused by a large contact resistance and a high sheet resistance.

This paper will address the status of AlGaN/GaN HBTs grown by MOCVD. The highly resistive base has been preliminarily addressed by both employing external base region regrowth and by investigating superlattice doping.

Experimental results of our multiple approaches will be presented and optimistic predictions provided.

GaN/SiC Heterojunction Bipolar Transistors

J. T. Torvik, J. I. Pankove, M. W. Leksono, Astralux Inc.
G. Eldridge, Northrop-Grumman Corp.
B. Van Zeghbroeck, University of Colorado at Boulder

We report on the evolution of the fabrication and characterization of high-temperature and high-power GaN/SiC n-p-n heterojunction bipolar transistors (HBTs). The HBT structures consist of an n-SiC collector, p-SiC base, and an n-GaN emitter. Initially, the HBTs were fabricated using reactive ion etching (RIE) to define the emitter and base areas. However, the poor etch selectivity between GaN and SiC made it difficult to stop at the thin base layer. Furthermore, the RIE caused damage at the heterojunctions which resulted in large leakage currents. Selective area growth was therefore employed to form the n-GaN emitters. GaN/SiC HBTs were first demonstrated using the 6H-polytype. These transistors had an extraordinary high dc current gain of $>10^6$ at room temperature of and were able to operate at 535°C with a current gain of 100. However, in more recent work this performance could not easily be reproduced due to the presence of a parasitic deep defect level in the p-type 6H-SiC. The possibility of obtaining higher quality 4H-SiC than 6H-SiC without this defect level seemed promising since much materials development is focused on 4H-SiC due to it's larger energy bandgap and superior electron mobility. Recent results will be presented showing GaN/4H-SiC HBTs with common base transistor operation with a modest dc current gain of 15 at room temperature and 3 at 300°C.

GaN NPN Junction Issues and Developments

Robert Hickman, Ph.D.
Blue Lotus Micro Devices
an SVT Associates Subsidiary

Critical nitride-based p-n junction issues relating to wide bandgap bipolar device performance will be examined. Required areas of improvement such as minority carrier lifetime, defect related current characteristics and base contact properties will be identified based on performance parameters reported for HBT and p-n junction research. Recent developments in improved junction materials processes will be reported. Included will be improved current characteristics using molecular beam epitaxy (MBE) on GaN buffers grown by metalorganic chemical vapor deposition (MOCVD). These GaN buffer results will provide some indication for the potential of various processes should GaN substrates become available.

GaN/SiC HBTs

William J. Schaff, Hong Wu, Choudhury Jayant Praharaj,
Michael Murphy, Brian Foutz, Oliver Ambacher and Lester F. Eastman
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Heterojunction Bipolar Transistors (HBT)s made from GaN emitter and SiC base and collector regions are desired for high power, broad bandwidth microwave amplifiers. In this work, several aspects of this device are addressed. The most critical element is the quality of the base-emitter junction. High efficiency emitter injection requires an interface between these lattice-mismatched materials which does not produce significant leakage current due to defects.

An important factor in understanding GaN/SiC heterojunction rectification is accounting for spontaneous polarization and piezoelectric effects. Theory will be presented which shows that a strained GaN/SiC junction will form a 2 dimensional hole gas in the base, while an ustrained junction will form a 2D electron gas. Different approaches to forming the emitter/base junctions are being conducted. The results of these investigations will be presented.

HBTs with microwave frequency layouts are in process. These multifinger transistors will be characterized with on-wafer probing of high frequency characteristics in addition to DC tests. Results will be presented.

Processing for GaN-based Heterojunction Bipolar Transistors

I. Adesida
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University of Illinois, Urbana-Champaign, IL 61801

There are many important factors to be considered in the realization of high performance GaN-based heterojunction bipolar transistors (HBTs). Epitaxial growth is a key consideration in the light of the low activation of p-type dopants in GaN. The low mobility and high resistance in the base section of the HBT structure are severe limitations on the performance of these devices. Another problem arising from the low activation of p-type dopants from processing point of view is the ohmic contact. In most published work to date, ohmic contacts on p-GaN are slightly rectifying. Etching is also an important processing consideration in the fabrication of GaN-based HBTs. Since the bonding energies of GaN and related materials are high, etching has been performed primarily with dry etching. Various forms of dry etching have been applied to pattern transfer in GaN. We will discuss these processes and their applications to the fabrication of AlGaN/GaN-based HBTs. The wet etching of n-GaN using a photo-assisted technique will be discussed along with its possible application to HBT fabrication.

GaN/SiC HBTs and Related Topics

Bart Van Zeghbroeck
University of Colorado at Boulder

GaN/SiC HBTs are promising high-power microwave devices because of the superior breakdown field, saturation velocity and thermal conductivity of silicon carbide. The wider bandgap of the gallium nitride emitter and the long minority carrier life time due to indirect bandgap of the silicon carbide allow the base to be thick and highly doped yielding a low base resistance. Challenges include the heteroepitaxy of a III-V semiconductor on a IV-IV semiconductor and the high defect density of silicon carbide. Devices fabricated on 6H and 4H silicon carbide have been reported, but a detailed understanding of the results has not been obtained.

In this talk, we will present a variety of I-V and C-V measurements obtained on GaN/SiC devices and discuss the related issues. These include the heterojunction band offset between GaN and SiC, the transport through the SiC base and the recombination mechanisms in the GaN/SiC heterojunction. The heterojunction band offset was obtained from C-V measurements on GaN/6H-SiC P-n junctions, yielding a 0.11 eV higher conduction band edge in the SiC compared to that of the GaN. The minority carrier transport was studied using lateral bipolar transistors, photodiodes and a bipolar transistor in which electrons are emitted through a thin oxide. Minority carrier lifetimes and diffusion lengths were extracted from different device structures and will be presented.

Prospects for Wide Bandwidth Transferred Substrate Power HBTs

Mark Rodwell, Umesh Mishra, Lee McCarthy, Peter Kozodoy
University of California - Santa Barbara

HBTs exhibit both higher power density than HEMTs. Output capacitance for a given power level is also lower, enabling higher bandwidths in broadband power amplifiers. High base sheet and contact resistance are major impediments to high HBT bandwidths in the AlGaN/GaN material system. Difficulties with base resistance can be greatly reduced by scaling the emitter and collector junction widths to c.a. 0.1 microns. In combination with recent advances in P-doping of AlGaN/GaN materials, high HBT bandwidths are feasible.

Prospects of Diamond Bipolar Devices

A. Aleksov, A. Denisenko, E. Kohn
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Diamond material parameters predict high performance high power and high temperature device. However up to now no technically relevant donor is available and the only acceptor is boron (EA-EV = 0.4 eV), which is only partially activated at room temperature. Therefore the main efforts in the past have been concentrated on p-channel FET structures. Still, the Fermi level can be moved into the upper half of the bandgap using nitrogen a deep donor, which is however not activated at room temperature (EC-ED = 1.7 eV). In addition, from UV diamond detector studies a hole diffusion length in the µm-range can be extracted. Thus bipolar transistor action of diamond devices may be also feasible. In this study bipolar transistor action was tested using p-n-p structures with nitrogen doped n-type base. The structures were grown epitaxially by MWPCVD. New non-rectifying contacts to the high resistive n-type base layer were developed using degenerately phosphorous doped silicon. The structures were tested in the common-base configuration. For the first time the bipolar action could be identified in a vertical epitaxial structure. Even at room temperature collector currents up to 1 µA were observed. The characteristics owever were totally parasitics dominated by a high base resistance (confining the current flow to the periphery) as well as by high leakage currents of the surface and base-collector junction.

Enhancement of Base Conductivity via the Piezoelectric Effect in AlGaN/GaN Heterojunction Bipolar Transistors*

P. Asbeck, E.T.Yu, S.S.Lau and W.Sun
University of California, San Diego

The implementation of heterojunction bipolar transistors in nitride-based material systems is hampered by poor base layer conductivity, which is attributable to a) large ionization energy of acceptor impurities, b) numerous compensation mechanisms that are typically present, and c) poor hole mobility (particularly in materials with large acceptor concentrations). "Doping" via the piezoelectric effect, in addition to conventional acceptor impurity doping, provides an attractive possibility for the improvement in base characteristics, since there is no acceptor ionization energy to contend with, and there is, in principle, no carrier scattering associated with the piezoelectric doping contributions. This paper discusses prospects for the improvement in base characteristics expected from "piezoelectric engineering".

Polarization induced by lattice-mismatch strain and spontaneous polarization are known to produce significant doping effects in AlGaN/GaN HFET structures, which can lead to sheet charge densities of the order of $10^{13}cm^{-2}$ at the AlGaN/GaN interface. With Group III-terminated (0001) AlGaN/GaN layers (corresponding to most MOCVD and many MBE-grown materials on sapphire substrates and on Si-terminated SiC substrates), the sign of the effective "piezoelectric doping" is positive, i.e. donor-like for AlGaN layers grown on top of GaN layers. To provide an acceptor-like contribution for Group III terminated surfaces, the GaN should be grown on top of AlGaN. This corresponds most naturally to the geometry of a collector-up device, in which the AlGaN acts as a wide bandgap emitter.

In this paper we discuss the potential base conductivity improvement from polarization effects, in conjunction with conventional acceptor doping and modulation doping. We also discuss the implementation prospects for collector-up AlGaN/GaN HBTs, including mechanisms for suppression of electron injection from regions of the emitter not covered by the collector (extrinsic emitter areas).

*This work is partially supported by ONR (Dr. J. Zolper).

The Values of Minority Carrier Lifetimes and their Implications for Bipolar Devices

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The wide bandgap semiconductors GaN and AlGaN show promise for applications in a wide range of bipolar devices. This include not only blue light emitting diodes and lasers, but also ultraviolet (UV) photodetectors and high power heterostructure bipolar transistors and thyristors. Material properties which significantly influence the design and performance of these devices are minority carrier diffusion lengths and recombination lifetimes. Minority carrier diffusion lengths and lifetimes have significant impact on efficiency of UV photodetectors, current gain of transistors and ON-state voltage of thyristors.

We report a direct measurement of minority carrier diffusion lengths for both holes an electrons by electron beam induced current. For planar Schottky diodes on unintentionally doped n-type and p-type GaN grown by various epitaxial growth techniques, the diffusion lengths were found to be (0.28±0.03) μm for holes and (0.20±0.05) μm for electrons. Minority carrier lifetimes of approximately 7 ns for holes and 0.1 ns for electrons were estimated from the measured diffusion lengths and mobilities. We attempt to correlate the measured diffusion lengths and lifetimes with several possible recombination mechanisms in GaN and establish a connection with the structural properties of GaN. We briefly discuss and compare our measurements and conclusions to existing theoretical and experimental results.

The impact of minority carrier diffusion lengths and lifetimes on performance of nitride based bipolar devices is demonstrated on the example of thyristor. In particular, the ON-state voltage, power dissipation and maximum current density of the nitride based thyristor switch are shown to significantly depend on the minority carrier (hole) lifetime.

This work was supported by DARPA and monitored by the ONR under Grant No. N00014-92-J-1845, and also supported by DARPA/EPRI and monitored by the ONR under Grant. No. MDA972-98-1-0006.

Design and Simulation of AlGaN/GaN Heterojunction Bipolar Transistors

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For the purpose of identifying an optimum nitride heterojunction bipolar transistor (HBT) structure, two-dimensional simulations of nitride-based HBTs have been performed using a MEDICI® code with 20,000 nodes, giving detailed two-dimensional device simulations. Further simulations have been performed using a semi-classical one-dimensional Monte-Carlo model to calculate the base transport properties of the devices.

The NPN HBT device structure we have simulated consists of an Al0.15Ga0.85N emitter, a GaN base, and a GaN collector. For comparison, graded-base devices with grading from Al0.05Ga0.95N at the emitter to GaN have been performed. Devices have been simulated with a base region of LB = 100nm, 75 nm, and 50 nm with all other device structural parameters remaining the same. In order to improve the transistor characteristics, it is common to try to decrease the base thickness. However, the best simulated device performance is obtained for the 75 nm graded-base device. For a 4 V bias across the 75 nm base, the saturation voltage is again around 5 V and the saturation current is increased to around IC = 1200 mA/mm. When the base bias is decreased, the transistor turns off quite sharply around 3.2V. The b is 1550 when the device is biased properly. From the Monte Carlo simulations, the base transit time for an Al0.15Ga0.85N/Al0.05Ga0.95N/GaN HBT having a 100 nm base thickness was calculated to be 5.0 ps and 3.0 ps for a 75 nm base width. The results agree with the Medici simulations. Additional results obtained from these simulations will also be described.

Materials Theory Based Modeling of Wide Band Gap Semiconductors: From Basic Properties to Devices

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In this talk we present a general methodology, materials theory based modeling, for predicting device performance in technologically immature materials that can proceed relatively independently of experiment. The models incorporated within this general approach extend from a fundamental physics based, microscopic analysis based on the band structure properties of the material to macroscopic, engineering based device models. Using this scheme, we have investigated the transport and breakdown properties of several emerging wide band gap semiconductor materials, i.e., GaN, InN, 3C-SiC, and 4H-SiC. The carrier drift velocities, mobilities, and impact ionization coefficients for these materials can be predicted using the materials theory based modeling method. Based on these results, device level simulations can then be made. Here we report Monte Carlo and advanced drift diffusion/hydrodynamic simulations of GaN based devices. The piezoelectric properties of GaN/AlGaN heterostructures are also reviewed and their usage as a new degree of freedom in device engineering is discussed. Specifically, we present a novel means of utilizing the piezoelectrically induced fields in strained GaN/AlGaN layers to alter the local electric field profile within the device structure. A new avalanching photodetector device scheme based on this principle is presented. It is found that the electron ionization coefficients can be strongly enhanced within this new structure by the action of the piezoelectrically induced fields. It is further suggested that this principle can be applied to improve the workings of GaN based HBT devices.

DC and High-Frequency Characteristics of GaN-based Heterojunction Bipolar Transistors

Dimitris Pavlidis, Egor Alekseev and Andreas Eisenbach

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The DC and high frequency performance of AlGaN/GaN SHBTs is analyzed using a drift-diffusion model and GaN/AlGaN material parameters, which were previously verified by modeling experimentally demonstrated device characteristics. The emitter-base diode turn-on voltage is a s high as 2.5V while the collector and base ideality factors were 1.2 and 1.6 respectively. A DC current gain of 93 is found at a collector current density of 5kA/cm^2 and the gain is maintained at this value up to about 20kA/cm^2. The devices show a small offset voltage of 0.5V. A forward breakdown voltage BV_{ceo} of 18V is found for designs with rather high collector doping of 4 x 10^{17}cm^{-3}. The current gain varies from 180 to 100 when the base doping is increased from 7 x 10^{17}cm^{-3} to 1 x 10^{18}cm^{-3}. At the same time the current-gain cutoff frequency f_T remained almost constant and equal to 10GHz while the maximum oscillation frequency f_{max} varied from 25 to 30GHz. By optimizing the transistor design and bias, an f_T of 18GHz and an f_{max} of 53GHz are predicted. Results of a time-domain, large-signal analyses are also presented to predict the power capability and efficiency of AlGaN/GaN HBTs.

GaN HBT Design and Optimization

Michael Wojtowicz
TRW Electronics & Technology Division
One Space Park, Redondo Beach, CA 90278

This talk will focus on the design and optimization of the emitter, base, and collector regions of GaN HBTs for power and high-frequency applications. Specifically, the impact of doping levels, band gaps, region dimensions, and carrier transport on the performance will be investigated. The final result is a GaN HBT profile that can meet a set of minimum performance requirements for use in existing power applications.

GaN offers high breakdown field, high carrier velocity, high thermal conductivity and excellent electron mobility. The advantages of the nitride family of materials have been demonstrated in the form of Schottky diodes, MESFETs, HEMTs and optoelectronic devices. However, GaN HBT development has been slower due to difficulties in realizing an efficient acceptor for p-type base doping. HBTs are normally used in power and high voltage applications so GaN HBTs would be readily implemented into these applications. These HBTs will enable the next generation of high power sources and power converters for insertions into existing commercial and military ground and space applications.

In order to realize an HBT that can be inserted into these types of applications they must meet a minimum set of performance requirements. Minimum oscillation frequency must be 20 GHz without impacting base sheet resistance or collector breakdown. The base resistance must be kept at 4 k½/square or less to reduce input losses without leading to emitter current crowding or reducing maximum oscillation frequency. A wide band-gap emitter must be used to realize high small-signal current gain without impeding current flow between the emitter and base. Design and optimization of the emitter, base, and collector regions are critical for achieving this performance and allowing GaN HBTs to be inserted into existing and future power systems.

SiC and GaN Bipolar Power Devices

T. Paul Chow
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Wide bandgap semiconductor devices, such as SiC and GaN, have many interesting material properties, like high thermal conductivity, high avalanche electric field, and high carrier saturation velocity, which have attracted them for high-voltage power switching applications. While many unipolar devices, such as Schottky rectifiers and field-effect transistors, have been demonstrated, there are fewer reports on bipolar devices, such as pin junction rectifiers, thyristors and bipolar transistors. In this talk, we will review the status of bipolar power device development in SiC and GaN, with particular attention on device structures and performance tradeoffs.

To quantify the performance enhancement possible with SiC and GaN, bipolar figures of merit has been proposed for pin junction rectifiers, thyristors and bipolar transistors. Among the bipolar transistors, we can classify them into two groups, those with odd number and those with even number of junctions. The BJT has an even number of junctions and hence its on-state voltage can be minimized through cancellation of junction voltages when it is in saturation. In this case, SiC clearly excels over Si over all switching frequencies and the power dissipation is smaller in SiC transistors. By contrast, the Insulated-Gate Bipolar Transistor (IGBT), which is the dominant silicon power transistor structure, has an odd number of junctions in its structure and its forward drop cannot be reduced to less than a diode drop. Since SiC has a large diode turn-on voltage due to its larger bandgap, its conduction loss cannot be less than the silicon device at low to medium current density and only yields a lower total power loss when the switching frequency exceeds a certain frequency, f_{min}. This f_{min}, at which the conduction loss is equal to the switching loss (at 50% duty cycle) is about 20KHz for SiC IGBT when compared to silicon. Another factor worth considerations is the dependence of the choice of bipolar over unipolar devices on the blocking voltage rating. Whereas the cross-over voltage for silicon is about 300V, that for SiC and GaN ranges from 2000 to 6000V and is also dependent on the operating temperature.

In contrast to silicon, both SiC and GaN have a higher hole ionization coefficient than electron ionization coefficient. Consequently, the bipolar device structures that are considered for SiC and GaN are different than those for silicon. For example, the npn bipolar transistor in SiC has a better BV_{CEO} than that of the pnp transistor. Also, since SiC has an indirect bandgap and GaN direct bandgap, the design for SiC bipolar transistors are close to silicon devices and GaN resembles GaAs devices.

The dependence of pin junction rectifier performance on minority carrier lifetime has been quantified and verified with experimental devices. Sufficiently low lifetimes in the drift region of the junction rectifiers result in a current-controlled negative resistance (CCNR) behavior. The performance difference between implanted emitter and epi-grown emitter on both junction rectifiers and thyristors will be discussed. Performance tradeoffs between complementary thyristor structures in SiC are evaluated. Thyristors in GaN is disadvantageous due to short diffusion length and poorer thermal conductivity of substrates.

Continued...

While the n-channel IGBT is the preferred Si MOS-gated bipolar transistor, the p-channel SiC IGBT has a better safe-operating-area (SOA) than the n-channel counterpart. However, another MOS-gated bipolar transistor (called MGT) structure is very competitive and has a larger reverse-biased SOA than both n- and p-IGBT's in SiC, as demonstrated with numerical simulations. Also, due to structural difference, the MGT is less sensitive to minority carrier lifetime in the forward drop vs. turn-off time tradeoffs than the IGBT. Due to short lifetime and lack of an acceptable MIS structure, the heterojunction bipolar transistor with AlGaN/GaN is more applicable for GaN-base bipolar transistors. Other heterojunction bipolar transistors involving GaN and various SiC polytypes on SiC substrates are also possible.

The author would like to acknowledge support from Office of Naval Research under Grant # N00014-95-1-1302 and DARPA under Contract # MDA 972-98-C-0001.

Characteristics of 10 kV Planar ACBTs in 4H-SiC

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Our first order analysis predicts lower forward voltage drop for 4H-SiC bipolar devices than 4H-SiC unipolar devices for breakdown voltages higher than 9900V. The maximum controllable current density and safe operating area of the Insulated Gate Bipolar Transistors (IGBT) fabricated either using the planar DMOS technology or the Trench MOS gate technology have been shown to be limited by the latch-up of the parasitic PNPN thyristor inherent in the IGBT structure. An IGBT in SiC has been fabricated, but is reported to have very poor characteristics due channel mobility of less than 0.001 cm_/V.s and a low breakdown voltage of 200 V ascribed to trench corners. Consequently, a planar Accumulation Channel Bipolar Transistor (ACBT) which takes care of the problems of low inversion channel mobility, premature oxide breakdown and parasitic thyristor latchup has been proposed at PSRC. In this paper, the electrical characteristics of a 10 kV planar ACBT in 4H-SiC will be presented and compared with those for a 10 kV silicon IGBT.

Two dimensional numerical simulations have been done for both devices using *MEDICI*. The 4H-SiC ACBT shows high saturation current density (6500 A/cm^2) at a low gate bias of 5V, with no latch-up. The FBSOA curves for the 4H-SiC ACBT show that the device supports almost 10,000 A/cm^2 upto 2500V at a gate bias of only 5V. With a lifetime of 1 ms, the on-state voltage drop of the 4H-SiC ACBT was 2.58 V at 100 A/cm^2, while that of the silicon IGBT was 22.7 V. The peak electric field in the gate oxide was below 3.5 MV/cm even at a high collector bias of 2000V, thus preventing the oxide rupture previously reported in trench structures.

SiC Gate Turnoff Thyristors for High Power, High Temperature Applications

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This paper presents an overview of SiC bipolar devices such as Gate Turn-Off Thyristors (GTO), MOS Controlled Thyristors (MTO), and NPN Bipolar Transistors. The paper also introduces a new power switching device configuration, namely, JFET Controlled Thyristor (JCT). It is the most promising near term SiC switching device given its high power potential, ease of turn-off, potential for 500°C operation and resulting reduction in cooling requirements. The device design, device processing, DC and switching characteristics, and scale-up issues are discussed for the basic SiC GTO structure. These devices (fabricated with inter-digitated, spoked and involute configurations) blocked up to 1000 V and had a forward voltage of 3.35 V (@ 500 A/cm^2) at 390°C. Turn-off times of < 200 ns have been measured for SiC GTOs conducting 3A forward current (corresponding to a current density of 1500 A/cm^2). Data on the GTO and MTO mode turn-off capability of devices with different geometry and gate-to-anode spacing will be included in the presentation In addition, high temperature packaging issues are addressed. An appropriate circuit model and a single phase inverter circuit are used to calculate the switching loss vs. switching frequency trade-off and comparison with silicon devices is presented.

Indepth Analysis of SiC GTO Thyristor Device Performance Using Numerical Simulations

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Taking advantage of silicon carbide's high-breakdown field strength, high-saturation electron velocity and high thermal conductivity, 4H-SiC gate turn-off thyristors promise very low on-state voltages, high off-state blocking voltages, and fast gate-controlled switching. Recent demonstrations indicate progress is taking place in this direction. In this presentation drift-diffusion model based steady-state and mixed-mode transient simulation results using the most recently measured material parameters will demonstrate trends for optimizing the 4H-SiC GTO thyristor structure. Accurate simulations of the I-V curve of measured devices will be demonstrated. Simulation results indicate that electrostatic field punch-through that reduces the off state voltage to 1/5 of that when punch through doesn't occur can be avoided if the n-base and p-buffer regions of the [anode / n-gated-base / p-drift-region / p-buffer / n-buffer / cathode] structure are doped above 5×10^{16} cm^{-3}. For a structure with an 8 μm thick p-drift region and p-buffer and n-gated base region concentrations in the range of 5×10^{16} to 4×10^{18} cm^{-3}, the blocking voltage doesn't vary by more than 10% from a median value of 1440 V. Increasing the n-base donor concentration reduces the maximum blocking capability while increasing the p-base dopant concentration increases it. However, the on-state voltage is strongly dependent on the concentration of both of these regions when they are doped above 1×10^{18} cm^{-3}. The minimum on-state voltage drop, V_{AKmin}, can be much above 4 volts when the n-gated base / p-buffer region concentrations (N_D / N_A) are near 4×10^{18} cm^{-3} (V_{AKmin} = 21.26 V for a structure with corresponding concentrations of $N_D = 1 \times 10^{18}$ / $N_A = 4 \times 10^{18}$ cm^{-3}.) Hole injection from the anode is reduced more strongly than electron injection from the cathode when the n-gated base and p-buffer regions have the same concentrations. Transient mixed-mode simulation results indicate that increasing the n-gated base concentration in general increases the turn-off gain.

Silicon Carbide Bipolar Power Devices - Potentials and Limits (2 parts)

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Power devices made with silicon carbide (SiC) are expected to show great performance advantages because SiC has an order of magnitude higher breakdown electric field and a 2-3X higher thermal conductivity than conventional semiconductors. To exploit the tremendous advantages offered by SiC for bipolar power devices, it is important to understand the relevant voltage/current range, fundamental limits and technological challenges in order to develop this technology commercially.

Fundamentally, unipolar devices made with SiC offer a lower on-state voltage drop (below 100 A/cm^2), an order of magnitude higher switching speed and a better high temperature stability as compared to bipolar devices up to a voltage rating of about 3000 V. However, the opportunity of operating a device at a higher current density (above 300 A/cm^2) to increase total current with reasonable yield, the poor reliability of MOS at high temperatures, and the relatively low channel mobilities obtained in 4H-SiC MOSFETs may make certain bipolar devices more attractive even as low as 1700 V. The upper limit on the blocking voltage is dependent on the ability to grow defect-free thick, low doped epitaxial layers on large area SiC. Recent improvements of the growth process using hot-wall CVD have improved the thickness uniformity over a 2 inch wafer to less than 1% and the doping uniformity to approximately 5%, both values expressed as s/mean, thereby making such epitaxial layers commercially available. Depending on the operating conditions, the maximum limit on the on-state current density may arise from one of the three factors: (a) the heat dissipation limit of the package (commercial packages limit the continuous current density to about 400 A/cm^2 at V_F=4.5 V); (b) the contact resistance of anode or cathode, especially if one of these contacts is p-type; and (c) the heat dissipation limit of SiC, arising only in very high pulsed current (>10^5 A/cm^2) applications.

Bipolar devices made with SiC offer 20-50X lower switching losses as compared to conventional semiconductors. Another very significant property of SiC bipolar devices is their lower differential on-state voltage drop than similarly rated Si bipolar device, even with an order of magnitude smaller carrier lifetimes in the drift region. This property allows high voltage (>20 kV) to be far more reliable and thermally stable as compared to those made with Silicon. The switching losses and the temperature stability of bipolar power devices depends on the physics of operation of the device. The two major categories of bipolar power devices are: (a) single injecting junction devices (for example BJT and IGBT); and (b) double injecting junction devices (like Thyristor-based GTO/MTO/JCT/FCT and PIN diodes). Detailed analysis of these devices will be presented at the conference.

Detailed measurements on devices with record breaking voltage and current ratings will be presented at the conference. These include 4H-SiC 6.2 kV PIN diodes, 2 A/5 kV PIN diodes, 605 V/1 A buried gate FCT and 20 mA p-channel IGBTs.

This work is supported by ONR contract number N00014-97-C-0271 and DARPA/ONR contract number N00014-98-C-0191.

Recent Development in SiC High Voltage Rectifiers

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In recent years SiC devices have been evolving from a mere vision to a serious alternative to silicon devices. Feasibility has been shown for numerous types of devices and new remarkable device results are presented in an almost continuous stream by many groups all over the world. With an emerging production technology the focus at present is shifting from demonstrating "best of all" results to reproducibility and increase of yield. Issues like reliability and cost are becoming the key issues.

With costs expected to be high in the beginning, niche market applications where silicon carbide offers substantial system benefits in terms of higher switching frequency and reduced power losses are expected to be the prime candidates to incorporate SiC devices. The main application there is in the power conversion area, where the development efforts on Si power switches (e.g. IGBT) put now very high demands on the free-wheeling diode. The reverse recovery charge of the diode is a major source of switching losses and the major limitation for the system performance today.

Various demands from the systems designers, e.g. the voltage range of the application, are best met by choosing different device concepts. In the low voltage range the JBS diode is a promising candidate. As a unipolar device, however, the JBS is not particularly well suited for high voltage applications due to the absence of carrier modulation, and the p-n junction diode there is the better choice. Additional requirements - such as surge current capability - will also speak in favor of the p-n-junction diode. In both cases, however, the switching losses generated by the reverse recovery charge of SiC diodes are only a fraction of those of a comparable Si device.

The reduction of margins (epilayer thickness, doping concentration, etc.) is a key factor in order to be able to utilize the superior power handling capabilities of SiC. From the systems side a fundamental requirement for paralleling of devices is equal current sharing under static and dynamic conditions. All those requirements put forth ever-increasing demands on the material specifications and their tolerances that have to be met by suppliers.

Related to reproducibility and reliability topics is the establishment of failure analysis techniques to separate process induced defects from those that are still present in the material, either substrate or epilayer. High leakage current and soft reverse characteristics can often be attributed to the presence of localized defects and it is important to identify their exact origin.

Fabrication and Characterization of 4H-SiC GTOs

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SiC gate turn-off (GTO) thyristor is a potential candidate for high power electric utility control applications. Thyristor structure is also a basic building block for other advanced devices such as field controlled thyristors that have potential DoD and civilian applications including motor control and HVDC transmission. The advantages of thyristor-based devices include high current and high temperature capabilities because of the conductivity modulation and high reliability of bipolar junctions at high temperatures.

In this talk, we will discuss the 4H-SiC GTO process technologies and measurement results. Switching measurements of 800 V GTOs with an anode current density up to 10,000 A/cm^2 will be presented. The turn-on and turn-off times will also be presented as a function of temperature up to 240 C.

Progress on SiC Bipolar Power Devices

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The purpose of this study is to develop devices for high temperature, high power motor control systems. In this study, ion-implanted SiC PiN planar power diodes were fabricated with junction areas of 6.25 x 10^{-4} cm^2 (250μm diameter), 6.4 x 10^{-3} cm^2 (800μm diameter), and 1.6 x 10^{-1} cm^2 (4000μm diameter) and SiC Gate-Turn-Off (GTO) Thyristors are currently in fabrication. Recent results on DC characterization and switching losses (turn-on and turn-off) for the SiC Schottky and a SiC ion-implanted PiN diode are presented and compared. The forward and reverse I-V measurements as well as the forward voltage drop at a given current density and reverse blocking voltage were examined at temperatures as high as 200°C. Reverse blocking voltages exceeding 3000V have been measured at room temperature. Switching tests at room temperature have also been performed. Comparison of turn-off switching losses were made between SiC, Si and GaAs PiN diodes Reverse recovery current was found to be approximately 50% less for the SiC PiN compared to the Si PiN at room temperature. It has been calculated that these SiC diodes will consume less than one tenth the energy of their Si counterparts. Measurements of these diodes at high temperatures and at higher voltages is currently underway. These initial results combined with the SiC GTO's show promise for the future of high voltage, high current motor control systems and pulsed power applications.

This work was supported by DARPA Contract Number MDA 972-98-C-0001.

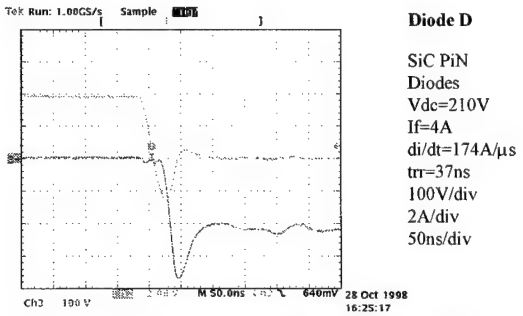

Fig. 1: Turn-off Switching Waveforms for SiC PiN diode at 25°C-If=3A, Vdc=170V.

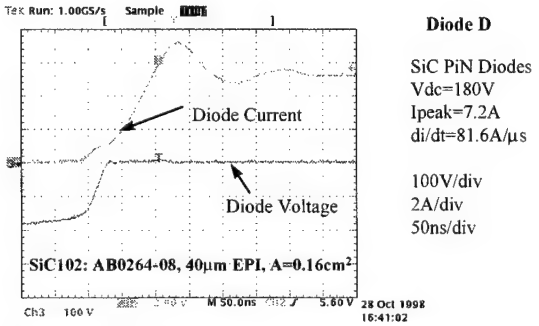

Figure 2. Turn-on Switching Waveforms for SiC PiN Diode at 25°C-If=7.2A, Vdc=180V.

Ohmic Contacts to p-Type GaN and SiC

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In this presentation, I will discuss work on ohmic contacts to p-GaN and p-SiC, briefly reviewing the literature and then describing results obtained in our own laboratory. For p-GaN, our experiments provide a comparison of a variety of single metal and bimetallic contacts deposited by sputtering, thermal and electron beam evaporation, and electrodeposition. When measured at room temperature, none of the contacts were perfectly ohmic; however, the most linear I-V characteristics by far were obtained following annealing of electrodeposited Pt and sputtered Ni/Pt contacts. This result was reproducible and was obtained on p-GaN from two different sources. An explanation for our findings will be put forward. For p-SiC, we will discuss reported ohmic contacts that have been demonstrated for very heavily doped p-SiC and point out which are still effective on less heavily doped material. Emphasis will be given to the Al-Ti, Ti, and refractory metal boride contacts that we have studied as part of a collaboration with researchers at Auburn University and Murray State University. Finally, we will discuss the surface and interfacial morphology of annealed contacts to both p-type semiconductors. The interfacial morphology in particular can be an important consideration when non-spiking contacts to a thin p-type semiconductor layer are required.

GaN Etching Techniques

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GaN can potentially offer a highly efficient and low cost solution for high power applications up to K-band, if epitaxial growth and general processing techniques can be improved. Dry and wet etching techniques of AlGaN/GaN based materials have matured tremendously over the past few years, but they must be refined to ensure a future of GaN in microwave and millimeter wave applications. This paper will discuss the thermodynamic properties of possible reaction mechanisms associated with typically used dry and wet etching techniques. The theoretical calculations presented here will provide a basis for experimental comparison in order to promote more understanding in the nature of AlGaN/GaN chemical etching.

Using standard enthalpy and entropy of formation values, the Gibb's free energy and the standard reduction potential for dry and wet based chemical reactions, respectively, can be calculated. These calculated thermodynamic values will predict the spontaneity of the reaction, although kinetic information can not be directly obtained. In particular, the standard reduction potential is the potential required to commence the chemical reaction, but the standard reduction potential does not include any surface depletion effects. The experimentally observed reduction potential is the addition of the standard reduction potential and the any depletion effects present at the surface. Using experimental and calculated reduction potential data, an estimate of the band bending at AlGaN or GaN surfaces can be obtained.

An Improved Inversion-Mode 6H-SiC DIMOS Power Transistor

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A basic limitation to the realization of planar SiC MOS Power Semiconductor Devices, such as the DIMOS (Double Implanted MOS Transistor), is the degraded electron mobility in inversion layers on heavily-implanted, oxidized p-type SiC annealed at high temperatures. The electron mobility plays a major role in determining the specific ON-resistance of these devices and therefore the internal power dissipation. The quality of the SiC-SiO_2 interface, the method to grow the overlying SiO_2, the ion type (i.e. Al or B) and activation of the implanted ions all play a role in determining the electron mobility. Our research is directed towards a study of electron mobility in inversion layers through the characterization of electron transport in novel surface and buried-channel Silicon Carbide MOS and DIMOS devices. We are interested in the basic limitations to the carrier mobility caused by the effects of the implantation, the growth of the gate oxide and the impact of high-temperature anneal operations. In this talk we describe some preliminary experiments performed with Al ion implantation for the p-well dopant and the P^+ contact to the p-well. The Al activation is performed at 1400C to reduce 'step-bunching', which occurs at elevated temperatures. The DIMOS devices employ deep N^+ implants into the vertical JFET region to inhibit constriction of the channel by the flow of current, thereby, allowing a higher current density at reduced pitch. The extracted room temperature electron mobility μ_n = 30 cm^2/Vs from lateral MOSFETs on the test pattern is the best reported to date for heavily-implanted p-wells. We believe this is due to the combination of a low temperature anneal (1400C) to reduce step-bunching, the use of Al for the dopant for more efficient activation at temperatures below 1500C, and the growth of a high quality gate oxide with reduced carbon incorporation at the SiC-SiO_2 interface. A non self-aligned, 2 μm channel length, 6H-SiC DIMOS structure with 5 μm p-well spacing, source length of 23 μm, deep N+ implants to suppress the JFET 'pinch' effect, a drift region of 10 μm with an overall cell pitch spacing of 32 μm exhibits a 400V 'punch-through' limited blocking voltage and a specific ON resistance $R_{on,sp}$(exp)= 42 mW-cm^2 at 300K with V_G = 20V (V_T = 4V), V_D = 5V in agreement with theoretical calculations and simulations. A non-implanted structure exhibits a $R_{on,sp}$ = 80 mW-cm^2 under the same test conditions. A blocking voltage of 1000V is possible with the above structure through optimization of the p-well profile. In addition, a reduced $R_{on,sp}$ may be obtained by minimizing the source region length (e.g. a source length of 5 μm would permit a two-fold reduction in the specific ON resistance). These results are already superior to silicon DMOS devices and with the addition of a self-aligned technology, demonstrate the potential of SiC DIMOS devices to make a significant impact in the area of power switching applications.

State-of-the-Art SiC MOSFETs as an Alternative to Bipolar Devices for Power Switching Applications

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The specific on-resistance of the drift region in unipolar devices scales as the square of the blocking voltage and inversely as the cube of the critical electric field. Since silicon carbide (SiC) has a critical field 8-10x higher than silicon, unipolar devices in SiC are theoretically capable of on-resistances up to 400x lower than silicon devices of the same blocking voltage. Unipolar devices are preferred over bipolar devices for high-frequency applications because they exhibit no reverse recovery transient, virtually eliminating switching losses that scale with frequency. For devices with moderate blocking voltage the on-state losses are also lower, since unipolar devices do not introduce a diode drop in the conducting state. For these reasons, SiC Schottky rectifiers are expected to displace silicon PiN diodes and SiC power MOSFETs are expected to displace silicon IGBTs in many system applications.

In spite of the previous statements, the specific on-resistance of SiC power MOSFETs developed to date has been limited by the resistance of the MOSFET channel, not by the drift region, and consequently the performance has fallen short of the ideal. The drift region resistance is inversely proportional to the electron mobility parallel to the c-axis. This mobility varies significantly with polytype: in 4H-SiC, the electron mobility is about 900 cm^2/Vs at typical dopings, while in 6H-SiC it is only around 100 cm^2/Vs. For this reason, 4H-SiC has been utilized for most vertical power MOSFETs to date. Unfortunately, MOSFET inversion channel mobilities have typically been much lower in 4H-SiC than in 6H. The MOSFET channel mobility can be significantly increased by converting a thin layer of SiC adjacent to the oxide to n-type, thereby forming an accumulation-layer MOSFET or "ACCUFET". UMOS and DMOS ACCUFETs were reported in 1997 by Denso and NCSU, respectively, and exhibited specific on-resistances of 10.9 and 18 $m\Omega\text{-}cm^2$ at blocking voltages of 450 and 350 V. In 1998, Purdue reported a UMOS ACCUFET with special features to protect the trench oxide from high electric fields. This device achieved a blocking voltage of 1400 V with an on-resistance of 15.7 $m\Omega\text{-}cm^2$, 25x lower than the silicon theoretical limit. This oxide-protected UMOS ACCUFET is expected to be competitive with silicon IGBTs in the 800-1200 V range.

This talk will review progress in SiC power MOSFETs and discuss current problems in the design and fabrication of these devices. New data will be presented on the effect of implant activation anneals on surface morphology, and the subsequent effect of surface morphology on MOS inversion channel mobilities in 4H-SiC.

This work is supported by ONR/MURI grant no. N00014-95-1-1302.

Advanced Heteroepitaxy of Silicon Carbide on Silicon

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Much research has been devoted to the heteroepitaxial growth of device grade silicon carbide, with an emphasis on the growth of the cubic polytype of silicon carbide (3C-SiC) on silicon as this approach would appear to have significant economic and technical advantages. However, the large (20%) lattice mismatch between 3C-SiC and <100> silicon has prevented device-grade 3C-SiC on Si to be realized. In this talk, we report recent results in chemical vapor deposition of 3C-SiC on twist-bonded "universal compliant" silicon substrates, including TEM micrographs and X-Ray topography, that indicate some improvements. Additional work is indicated to reduce the 3C-SiC deposition temperature and to develop next generation compliant substrates to reduce the overall lattice mismatch that must be accommodated. Ideas include ternary pseudo alloys of silicon, germanium, and carbon to increase the lattice constant relative to silicon carbide (such as has been demonstrated by implanting germanium into silicon carbide). Applications for HBT's are discussed.

Electrothermal Analysis of SiC Power Devices Using Physically-Based Device Simulation

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Silicon carbide (SiC) receives strong attention for high power device applications because of its promising material properties. The wide band gap, larger by a factor of 2.5 - 3 compared to silicon, and the excellent thermal conductivity allow to operate SiC bipolar devices under high temperature conditions, with a maximum temperature nearly three times above that of silicon. As the breakdown field strength exceeds that of silicon by a factor of nearly 10, we also obtain a much higher blocking capability of reverse-biased pn-junctions. Hence, when designing a power device, we may either increase the blocking voltage or we may reduce the device thickness, leading to a significantly smaller on-resistance and better switching behavior compared to state-of-the-art silicon devices.

However, with a view to optimizing the device performance, the realized test–structures and prototypes still require a much more detailed understanding of their internal physical behavior in the various regimes of the operating area. To this end, we formulated an extended electrothermal transport model covering most of the physical effects relevant to SiC devices. This includes, among others, various field-dependent generation-recombination mechanisms specific of wide-gap materials and their impact on the blocking capability, the consequences of anisotropic carrier mobility, and the effect of trap dynamics and dynamic impurity ionization on fast switching transients. Numerical device simulation based on these models allows to visualize the "internal life" of a device and, hence, to draw conclusions for an improved device design.

Comparing 4H-SiC Power Switching Devices: UMOS, Hybrid JFET, GTO and NPN Transistor

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This paper presents a comparative overview of 4H-SiC switching power devices: UMOS, hybrid JFET, GTO and NPN transistor at 4.5-kV level by theoretical analyses and extended two-dimensional numerical simulations. The channel conduction loss of the 4.5-kV UMOS is very small compared with the drift region loss. Comparing with the SiC GTO, the SiC UMOS has smaller conduction loss at current densities lower than 250 A/cm^2. Hybrid SiC JFET is a normally off power switching device that takes advantages of SiC material for high-power and high-temperature, and low-voltage, large-current silicon MOSFET for MOS control. The hybrid SiC JFET has similar conduction loss as the SiC UMOS at current densities lower than 200 A/cm^2. Gate turn-off thyristor is another popularly studied SiC power switching device. Its latching characteristic results in very small voltage drop increase after it enters its latching state. Therefore, the SiC GTO has the advantage at high-current density applications. However, theoretical analyses show that the thermal resistance of device packaging limits the maximum useable SiC GTO's current density to below 500 A/cm^2. The voltage required to overcome the junction barrier voltage (about 2.9 V for 4H-SiC) is the dominant loss in the GTO. Bipolar transistor eliminates this major disadvantage and can have a forward voltage drop of as low as 0.2 V with a reasonable current gain of ten. Simulations show that 4.5-kV SiC NPN transistor has the lowest conduction loss in all studied SiC power switching devices.

Status and Prospects for SiC SITs

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Silicon Carbide SITs are a family of majority carrier devices that rely on a mixture of field effect transistor operation at high currents and space charge injection over a gated barrier at high voltage. These transistors show currents as high as 1-5A/cm and blocking voltages in excess of 350V. With this extremely large power triangle it is possible to build parts with a power density in excess of 100KW/ cm^2. For example pulsed SIT packages have shown 450W output power at L-band with 58% efficiency, and S-band packages have developed 240W with 30% power added efficiency.

In this talk new "ion implanted gate" 4H-SiC L-band SITs will be described outlining their advantages for rugged, high power generation and reduced cost. Future SIT designs for operation at frequencies of 5GHz will be explored and the potential for extremely high power CW SIT operation will also be examined.

Fabrication of 300°C GaN/AlGaN Heterojunction Bipolar Transistors

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This talk will report on the large area GaN/AlGaN heterojunction bipolar transistors recently fabricated using a combination of Cl2/Ar ICP dry etching with a wet chemical clean-up for reduced damage mesa formation. Both MOCVD and MBE have been used to successfully grow the active portions of the device, though in the case of MBE an initial 2 mm nucleation layer grown by MOCVD was required. The advantages and disadvantages of each method with regard to control of the composition and morphology will be presented. For both growth techniques, large area devices show improved gain above 250°C as the hole concentration increases due to more efficient ionization of the Mg acceptors at elevated temperatures (> 250°C). At 300°C a gain of 10 is obtained, though the device performance is still limited by the base doping. Various approaches which appear promising for improving the base resistance, such as regrowth of the extrinsic base, will be discussed. Additional problems associated with GaN HBT development such as precise placement of the base emitter junction, and minimum achievable doping levels in the collector will also be discussed.

GaN Growth on Lithium Gallate Substrates

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Recent analysis of the structural and electronic properties of GaN on the alternative substrate, lithium gallate ($LiGaO_2$ or LGO), shows great promise for the development of high performance microwave devices using GaN/LGO. The GaN/LGO system possesses a relatively small lattice mismatch of 0.19%, leading to improved structural properties for relatively thin films in comparision to GaN on sapphire. Undoped AlGaN/GaN heterostructures on LGO show relatively high two-dimensional electron gas (2DEG) conductivities. In addition, LGO is easily removable from the GaN after growth. This should enable advanced packaging techniques for improved heat removal for high power, high temperature devices.

We will report on the growth of GaN on LGO by Molecular Beam Epitaxy. The properties of GaN on LGO that relate to bipolar development will be covered. These issues include the growth of AlGaN/GaN and InGaN/GaN heterostructures, the extent and consequences of Li outdiffusion, and initial Mg doping experiments.

Two Dimensional Hole Gas Induced by Piezoelectric and Pyroelectric Charges

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The pyroelectric and piezoelectric effects play an important role in AlGaN/GaN/InGaN based heterostructures. [1-3] Very high values of the two-dimensional (2D) electron sheet density (up to $3x10^{13}$ cm^{-2}) have been both predicted theoretically and demonstrated experimentally in AlGaN/GaN Heterostructure Field Effect Transistors. Recently, it was suggested that piezoelectric effects could induce the 2D-hole gas. [4] We will present the results of the band structure calculations for a gated AlGaN/GaN heterostructure with undoped AlGaN layer and a lightly doped p-type GaN layer. These calculations are based on the analytical self-consistent solution of the Poisson and Schrödinger equations at the heterointerface and on the calculations of the spontaneous and piezoelectric polarization as functions of the lattice mismatch based on the theory of elasticity. The results confirm that piezoelectric and pyroelectric charge can induce the 2D-hole gas at the AlGaN/GaN heterointerface. The densities of the 2D hole gas exceeding 10^{13} cm^{-2} can be obtained in a p-type or even in nominally undoped GaN. (Our calculations show that in an n-type GaN, the hole 2D-gas might be very difficult to induce.) The metal/AlGaN/GaN band structures have been calculated for different doping levels with and without accounting for the effects of spontaneous polarization. The results suggest that piezoelectrically induced 2D-hole gas can be used for the reduction of the base spreading resistance in AlGaN/GaN-based Heterostructure Bipolar Transistors.

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Materials Challenges for p+ SiC-based GaN/SiC HBTs

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Wide bandgap heterojunction bipolar devices (HBT) are being investigated primarily because of their inherent linearity and projections of high power at microwave frequencies. SiC-based HBTs offer possible advantages over GaN-based HBTs in performance mainly due to the relative ease of producing highly doped p-type material and making Ohmic contacts with $< 10^{-5}$ ohm-cm^2 contact resistance to this material. Initial work using SiC-based HBTs showed great promise [1], but no true microwave performance has yet been achieved. More recent attempts at SiC-based HBTs exhibited electron traps that reduced gain and rendered devices unusable. These traps are located in the epitaxial p-type SiC material used in the base [2]. Our efforts have been focused on eliminating the electron traps located 1.25eV above the valence band by using the SiC epitaxial capability under development at Sterling Semiconductor. To determine the cause of these deep level traps, we are investigating the difference between the behavior of 4H- and 6H-SiC homojunctions, as many deep level impurities such as V and Fe behave differently in the two polytypes. We are also attempting to minimize background doping prior to p-type intentional doping, as this should also minimize the concentration of the killer traps. We have demonstrated less than 1×10^{15} cm^{-3} background doping as well as p-type doping in excess of 1×10^{18} cm^{-3} using Al as p-type dopant in both 4H- and 6H-SiC. Our current capability to eliminate this defect in p-type material will be discussed.

This work is supported by BMDO/ONR (Contract N00014-98-M-0136) and is monitored by J. Zolper.

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GaN/SiC Heterostructures Grown By LP-CVD

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Heterojunction bipolar transistors (HJBT) on the basis of GaN/SiC heterostructures, for which SiC can also be used as substrate material, have several advantages compared with group III nitride heterostructures grown on sapphire. For example there is no problem of optical recombination in a highly doped base region as there is for the group III nitrides in account of their direct bandgaps.

But in spite of the well acknowledged potential of this GaN/SiC material system there are still open questions related to technology as well as to some fundamental properties of GaN/SiC heterostructures. Therefore we investigated epitaxial growth and physical properties of n-GaN/p-SiC heterojunctions due to their significance for a n-GaN/p-SiC/n-SiC HJBT.
We grew n-type GaN ($n = 10^{18}$ cm^{-3}) on p-type SiC substrates ($p = 2 \cdot 10^{18}$ cm^{-3}) by an approach, which is similar to the usually used HVPE, in a horizontal hot wall reactor. Instead of synthesising GaCl in situ from HCl and metallic Ga we used $GaCl_3$ as Ga precursor. All our experiments are carried out at low pressures around 1 mbar resulting in a good homogeneity. As it is common for the more usual HVPE we grew without a bufferlayer.
From thermal and optical admittance spectroscopy as well as temperature dependent I-U characteristics we got knowledge about the bandoffsets and the role of interface traps. The microstructure of the interface was investigated by transmission electron microscopy (TEM). Furthermore we present some details about device processing by ion beam sputter etching with carbon dioxide as a working gas.

Growth and Applications of Thick 3C-SiC Films on Si

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One of the factors that has inhibited development of SiC device technology is the absence of large area and low cost SiC substrates. This has motivated the investigation of heteroepitaxial growth of SiC on Si in order to provide alternative substrates of SiC for electronic devices, X-Ray masks, MEMS devices, etc.

We have investigated the high rate growth of SiC films on large area Si substrates by CVD using the single precursors trimethylsilane (TMS) and silacyclobutane (SCB). Single crystal films have been obtained both on Si(100) and Si(111) substrates. We have determined the effect of various growth paramaters, including temperature, flow rate, pressure, use of a pre-growth carbonization layer. The SiC growth rate was found to increase significantly with temperature and flow rate for both 3MS and SCB. For example, SiC growth rates larger than 30 μm/hr have been produced using 3MS on Si (111) substrates. These growth rates obtained are much higher than those obtained using the conventional two precursor approach (silane and propane) or other single precursors like trichloromethylsilane, methyltribromosilane, etc.

We have recently initiated the in-situ doping of SiC films. N-type doping using nitrogen shows that the SiC mobility is inversely proportional to the doping level. For low-doped films, we have obtained a mobility of 350cm^2/V-sec for a carrier concentration of 4x10^{16}/cm^3.

These results indicate that SiC films grown on Si have the potential to produce large area, low cost alternative for various SiC device applications, ranging from power devices to MEMS switches.

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The Characterization of GaN and SiC Materials for Minority Carrier Device Applications

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While rapid progress has been made in majority carrier, wide band gap devices, minority carrier based devices have experienced slower development. Key to further development is a good understanding of p-type doping issues, minority carrier lifetime, and the variation in lifetime with injection level. Minority carrier lifetime measurements have been performed in a variety of materials including bulk and epitaxial 4H silicon carbide. Several techniques including non-contact photoconductive decay, low temperature/deep energy deep level transient spectroscopy, electron beam induced current and electron beam induced current-diffusion length mapping have been used. Comparisons will be made to previous results from time resolved photoluminescence measurements with emphasis placed on the accuracy of predicting real device performance. Discussions of the impact of various defects including dislocations, triangular defects, and shallow verses deep energy impurities will be presented. The impact of limited activation of p-type dopants will be presented as well as the role of defects in limiting breakdown voltages. Examples of high quality MBE grown nitride devices structures on alternative substrates will also be presented.

Opportunities for Wide Bandgap Bipolar Devices in Navy Systems

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Future Naval systems will require improved capabilities in low frequency power distribution and microwave frequency power generation. To date, the former has been served by silicon based components and the later has employed GaAs or InP based technologies. The conventional approaches are reaching their fundamental material limits and new methodologies based on wide bandgap semiconductors, namely SiC and AlGaN, are poised to be meet future systems needs. Within these applications both unipolar and bipolar devices will play a role. The opportunities for wide bandgap bipolar devices are described below.

The selection between unipolar and bipolar devices for power distribution rests primarily on the requirements for blocking voltage, forward voltage drop, and switching speed. Unipolar devices generally have a linear increase in the forward voltage drop, or on-resistance, with increasing blocking voltage due to the dominant component of the drift region resistance. Bipolar devices have a constant forward voltage drop controlled by the p/n junction turn-on voltage and the ability to achieve high levels of conductivity modulation in the drift region. This means there is a voltage above which a bipolar device will have a lower forward voltage drop, or on-resistance, than a unipolar device. The lower on-resistance translates to lower switching losses and higher system efficiency. For silicon technology this voltage cross over is near 100 V while for SiC technology, depending on the achievable material parameters such as minority carrier lifetime, this is at 3000 V or above. Significant Naval and commercial utility applications, such as pulse power and utility power distribution, exist in this high voltage regime thereby making bipolar switching desirable.

While the systems issues for microwave power generation are distinct from those for power distribution addressed above, the device level issues (doping, carrier lifetime, band discontinuities, etc.) are the same for both technologies. The attraction of bipolar devices, or more specifically heterojunction bipolar transistors (HBTs), at microwave frequencies is the potential for lower phase noise, higher linearity, and higher power density than field effect transistors. In particular, reduced phase noise is important for radar applications to improve the system sensitivity. Improved linearity is critical for future multifunction electromagnetic systems where multiple simultaneous signals will be handled by a common amplifier. Details of the microwave system needs and device considerations will be given at the workshop.

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Air Force Needs: The Technical Challenges of Wide Bandgap Bipolar Devices for Air and Space Sensors

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The next generation of sensors will require novel technological solutions to address the warfighters' needs in the air and space arena. These sensors will encounter harsh environmental conditions associated with thermal and radiation effects, while simultaneously providing enhanced dynamic range, bandwidth, output power, and efficiency. The potential solutions will be further constrained due to mass, volume, and cost. For example, sensors deployed on unmanned autonomous air vehicles (UAVs) and satellites must work with limited prime power, reduced mass and volume, and reduced environmental control. For UAVs these sensor enhancements yield longer time-on-station and additional sensitivity. For space-based applications with wide temperature variations and high levels of radiation, these improvements reduce launch cost, expand on-orbit functionality, and extend lifetime.

The development of wide bandgap (WBG) bipolar devices will enable significant advancements required to realize these novel sensors. WBG materials, such as GaN and SiC, can provide higher power density, elevated temperatures of operation, and more tolerance to radiation. While most device research based on WBG materials has focused on field-effect transistors, bipolar devices offer many unique advantages. For example, these advantages include higher breakdown voltages, wider bandwidth operation, compactness, higher efficiency, lower phase noise, better linearity, and less stringent lithography.

However, the development and application of WBG bipolar devices with these desirable characteristics for air and space sensors present many technical challenges. For example, the devices require p-type material with high conductivity and high minority-carrier diffusivity. Whereas, the compactness of bipolar devices and their associated thermal resistance require accurate electrothermal models to adequately optimize the devices for power amplifiers. These and other technical challenges will be discussed as they apply to future air and space force applications.

Roadblocks to Wide-Gap Bipolars

Colin E.C. Wood, ONR

This presentation will briefly depict R&D programs in-place, advances and remaining challenges before theoretical performance of high power HBT, and related minority carrier device are demonstrated in SiC & III-N semiconductors.

As in all bipolar transistors, materials-related *sine quam non*.include:

- high, controllable **P- and n-type doping
  - low parasitic base-access resistance.
  - low contact-resistance
- e-b hole-barrier >0.1eV
  - to prevent parasitic base-current
- **electron lifetime (te) >> base-transit time (tb)
  requires indirect-gap base, and /or e-b 'hot-electron' injection DEc
  limits base width, high power uses demand more:
- high breakdown voltage **Vb for large b-c voltage swing, which requires
  high impact ionization energy,
  **very low extended and deep-level defect density
- low on-resistance, high e-c current which requires
  low effective carrier mass => mobility
  high minority carrier saturation velocity Vsat.
- **Insulating and high thermal conductivity substrate

In addition there are there are several technological / processing issues such as: selective etching, contact materials isolation / termination etc.

Many desirable properties are intrinsic to WB semiconductors, others can only be achieved by 'end-runs' and some still challenge our innovation.

ONR is investment is targeting most of challenges above, with special emphasis on those designated **.